

The diagram shows a system with three main components: a CPU (1), a PULSE GENERATING SECTION (2), and a PULSE DIVIDING SECTION (3). The CPU (1) sends a "SET VALUE CHANGE" signal to both the PULSE GENERATING SECTION (2) and the PULSE DIVIDING SECTION (3). The PULSE GENERATING SECTION (2) produces an "OUTPUT PULSE" and also sends a signal to the PULSE DIVIDING SECTION (3). The PULSE DIVIDING SECTION (3) sends an "INTERRUPTION REQUEST" signal back to the CPU (1).

FIG. 2A

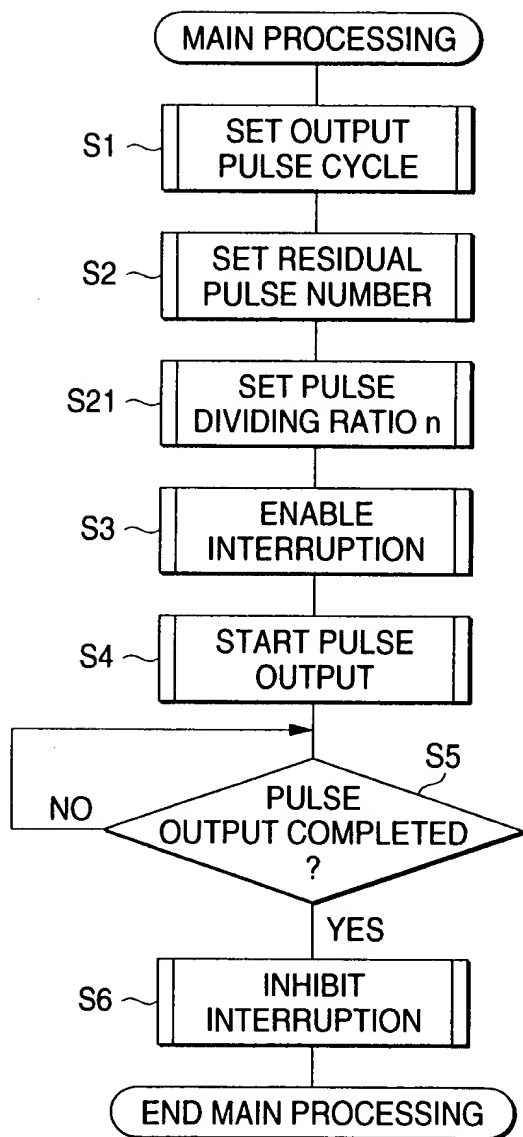


FIG. 2B

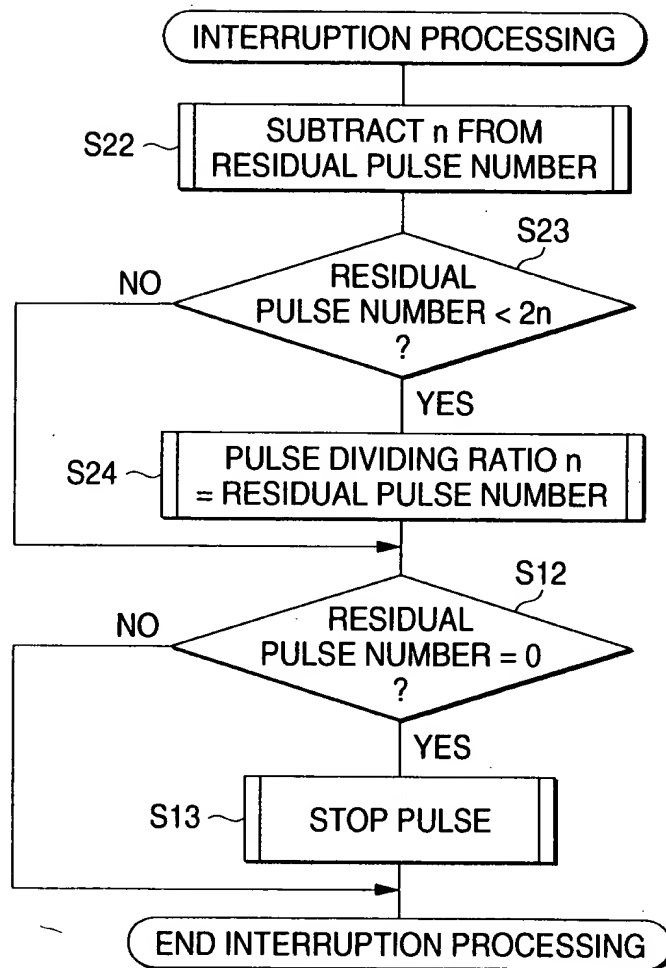


FIG. 3

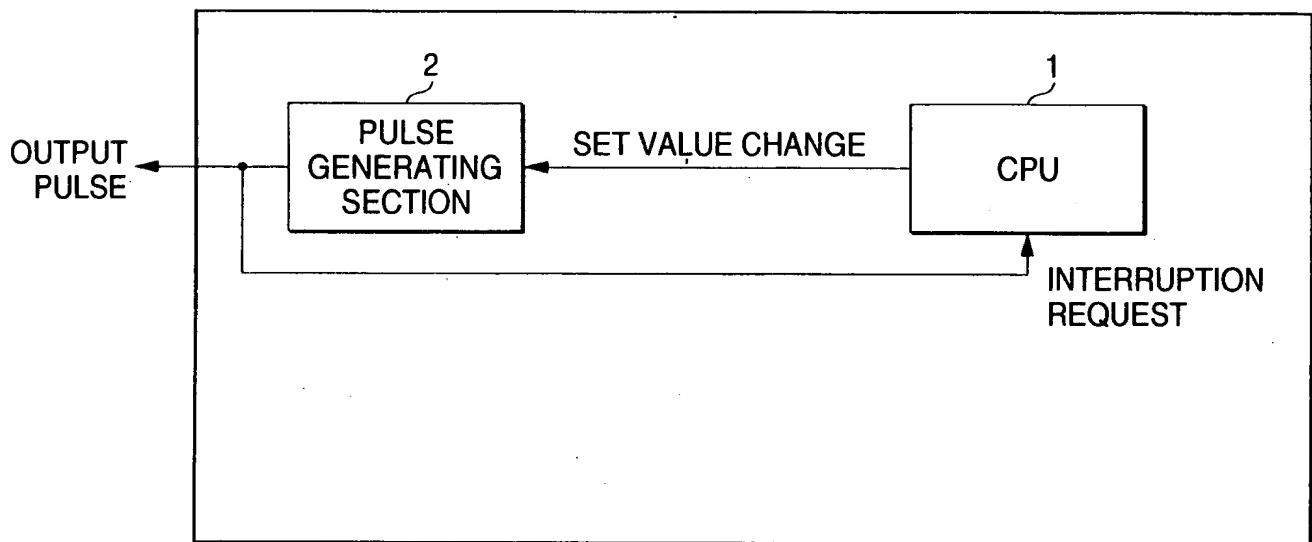


FIG. 4A

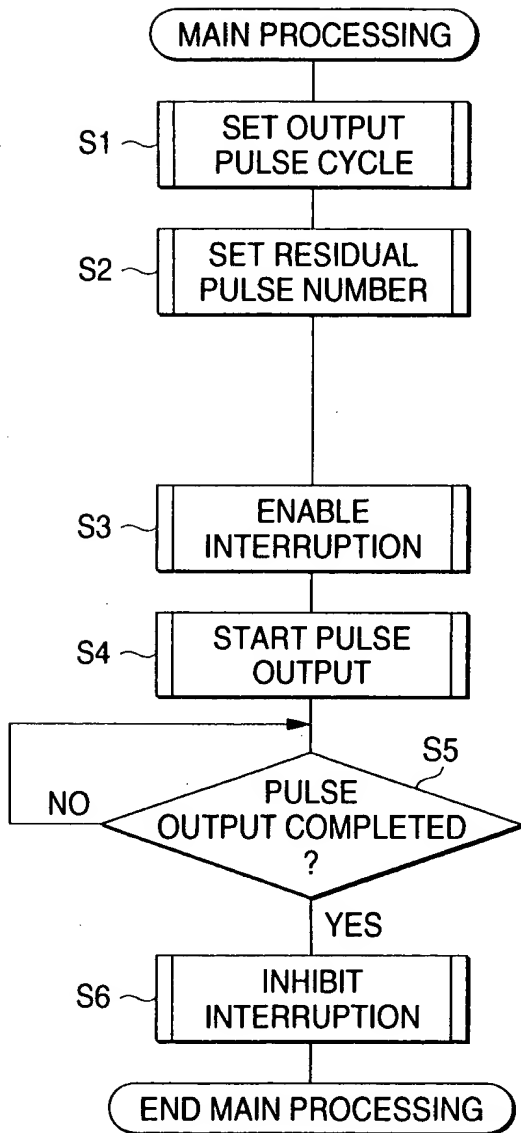


FIG. 4B

